OIPE
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PATENT & TRADEMARK OFFICE

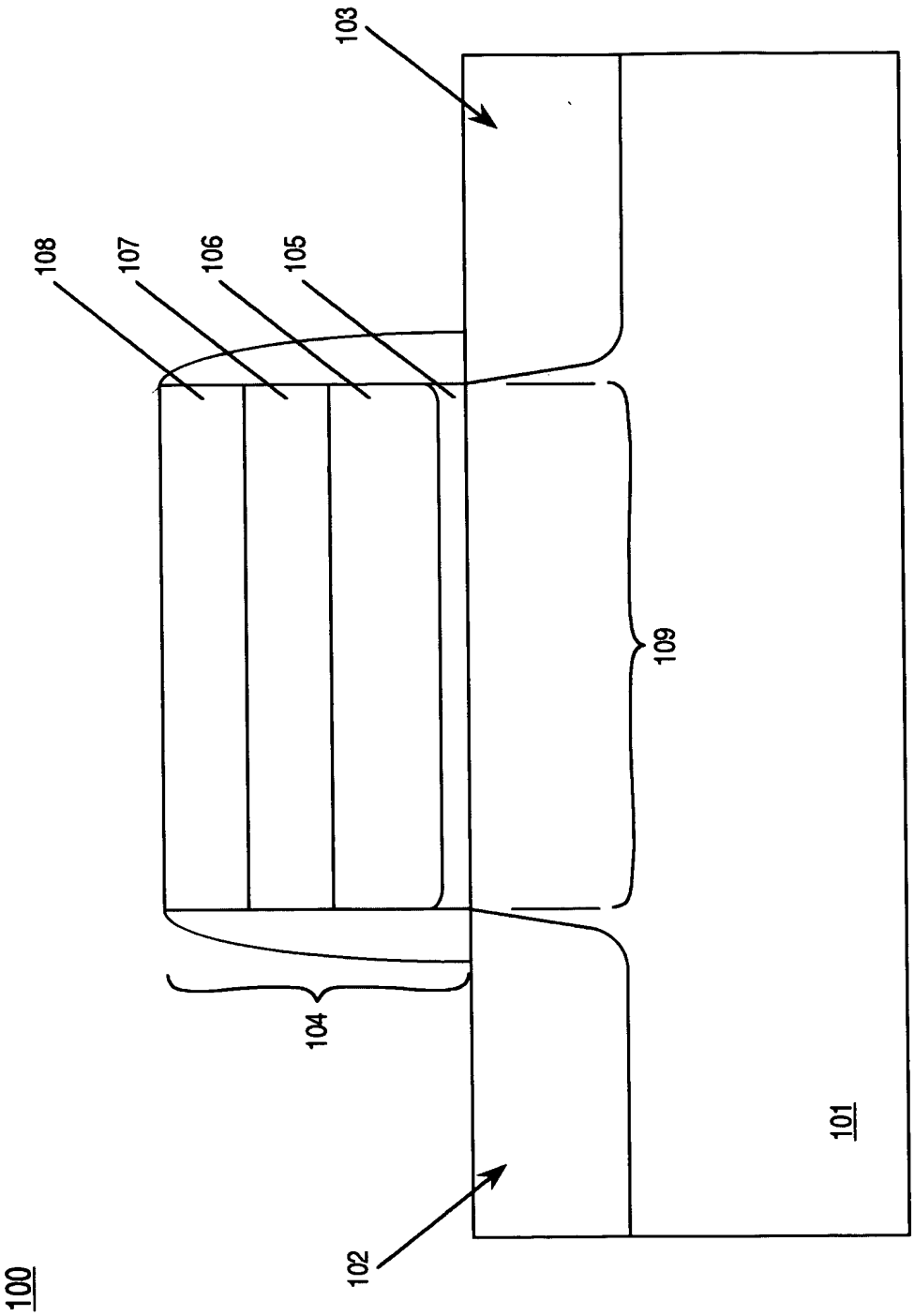

FIGURE 1
(PRIOR ART)

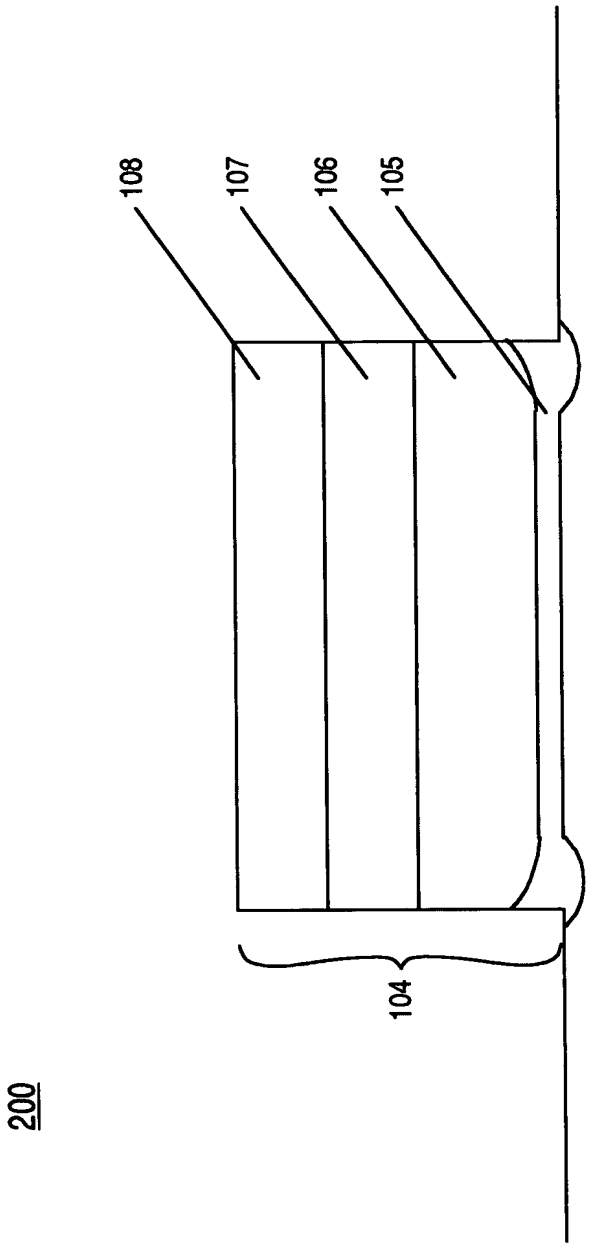

FIGURE 2
(PRIOR ART)

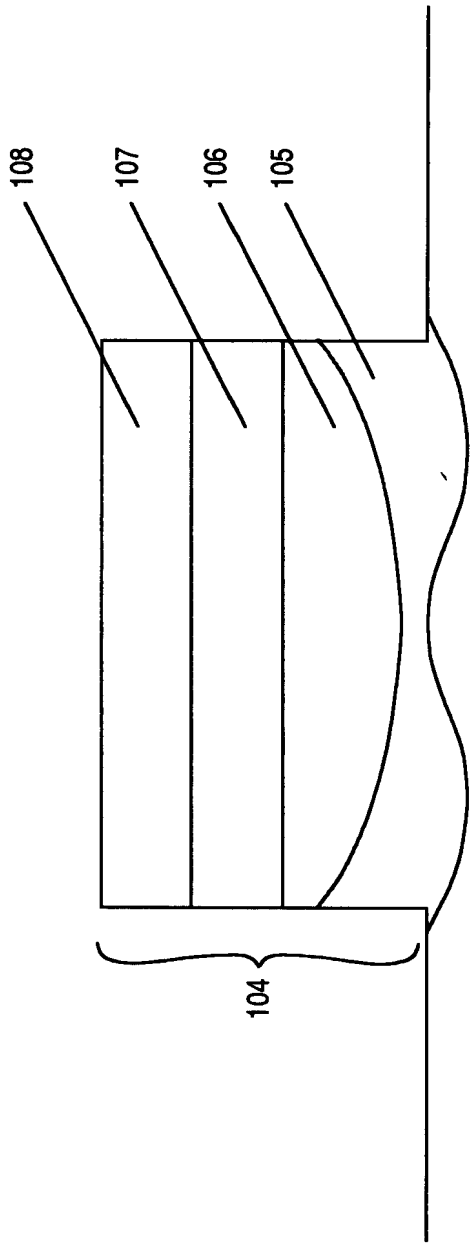

FIGURE 3
(PRIOR ART)

400

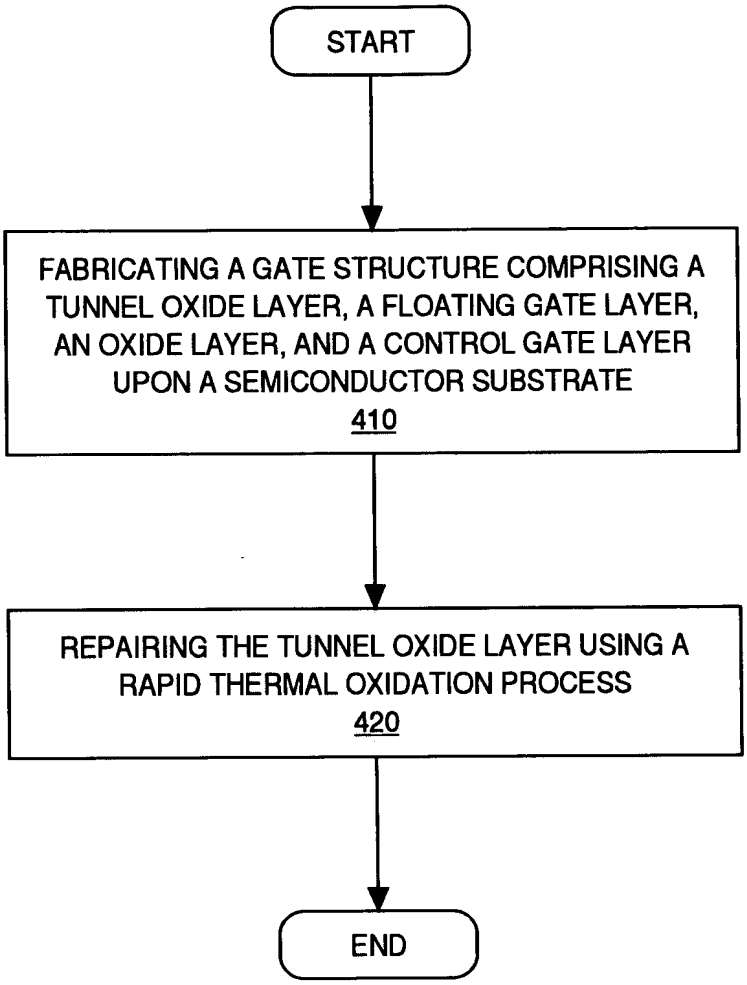
START
FABRICATING A GATE STRUCTURE COMPRISING A TUNNEL OXIDE LAYER, A FLOATING GATE LAYER, AN OXIDE LAYER, AND A CONTROL GATE LAYER UPON A SEMICONDUCTOR SUBSTRATE
410
REPAIRING THE TUNNEL OXIDE LAYER USING A RAPID THERMAL OXIDATION PROCESS
420
END

FIGURE 4

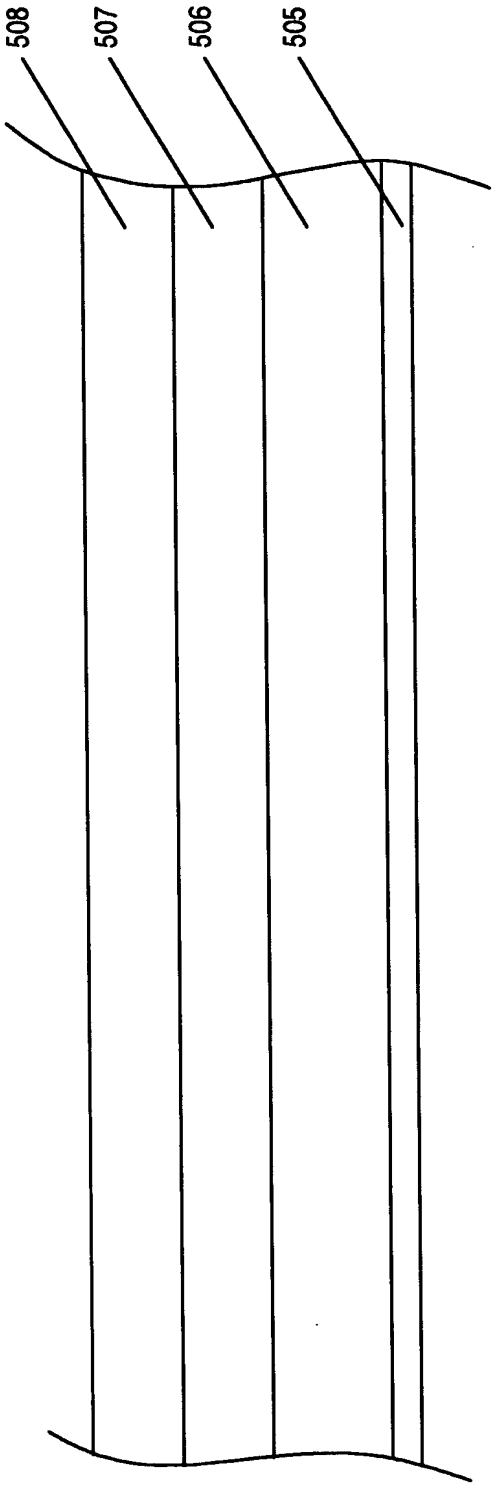

FIGURE 5A

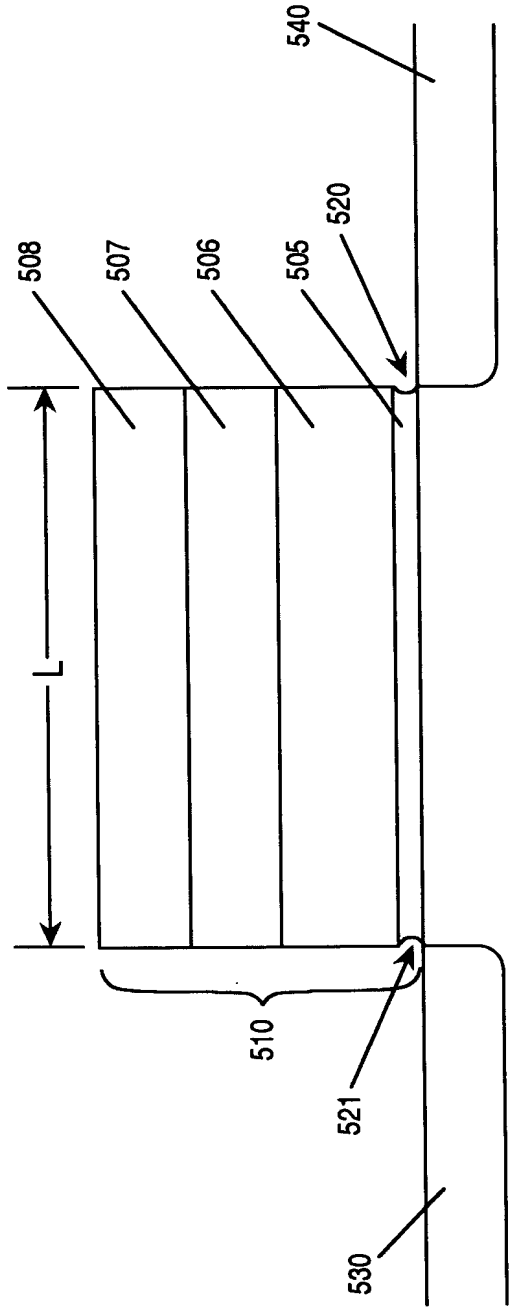

FIGURE 5B

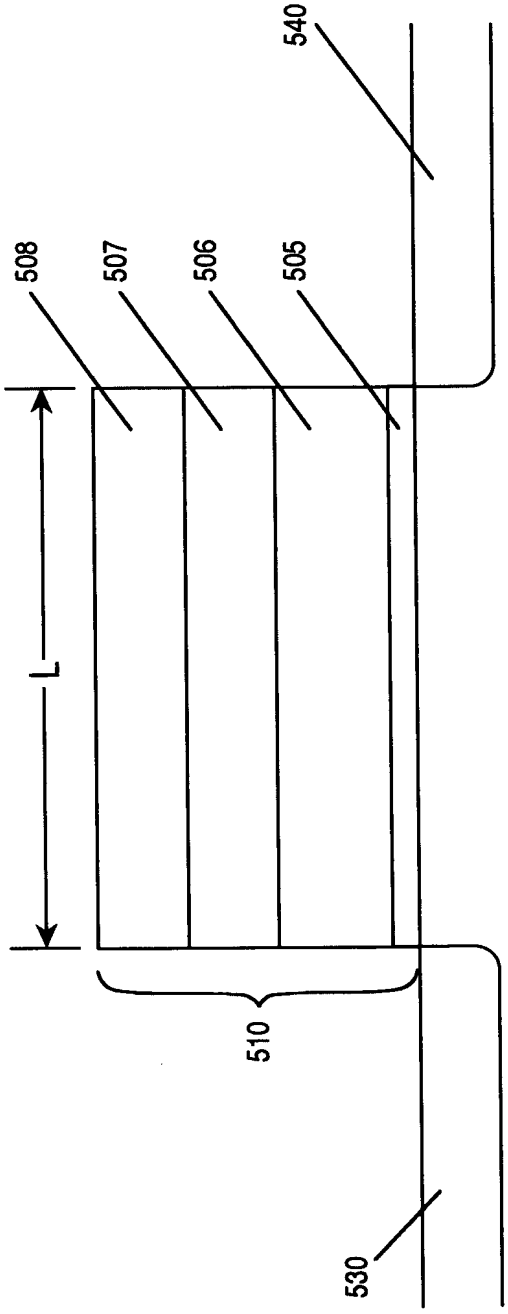

FIGURE 5C

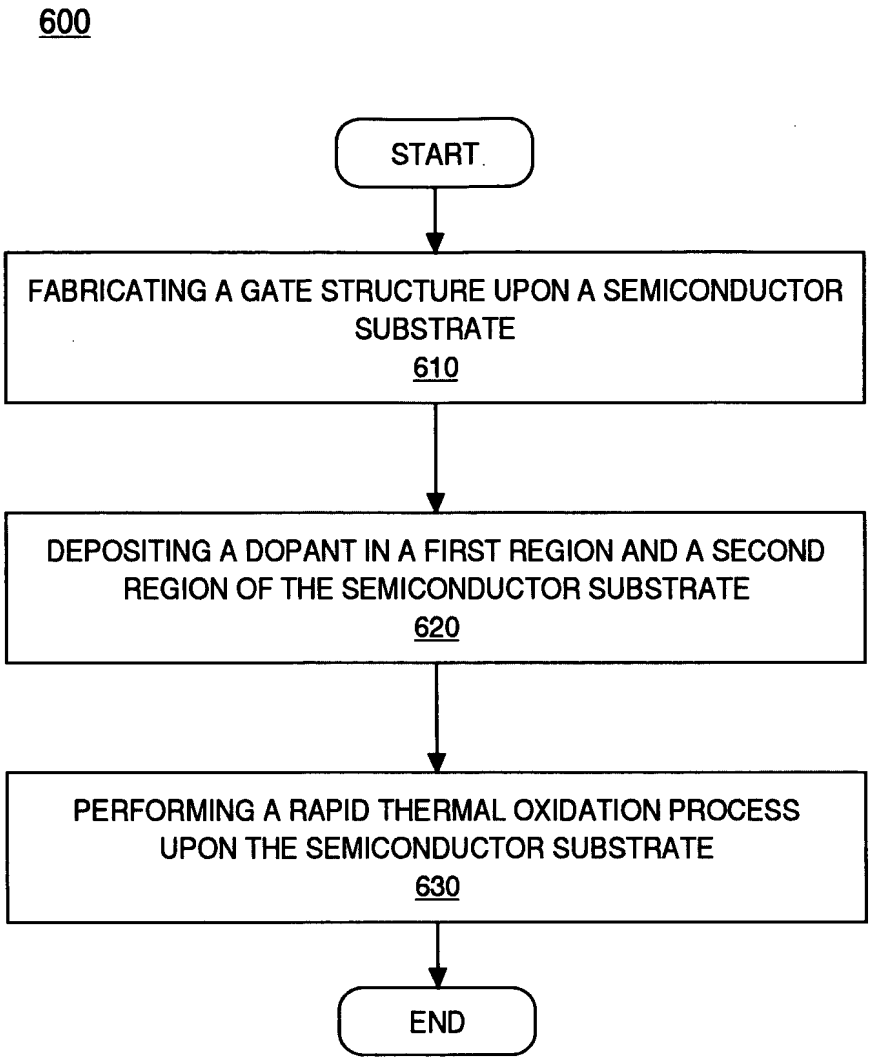
600
START
FABRICATING A GATE STRUCTURE UPON A SEMICONDUCTOR SUBSTRATE
610
DEPOSITING A DOPANT IN A FIRST REGION AND A SECOND REGION OF THE SEMICONDUCTOR SUBSTRATE
620
PERFORMING A RAPID THERMAL OXIDATION PROCESS UPON THE SEMICONDUCTOR SUBSTRATE
630
END

FIGURE 6

700

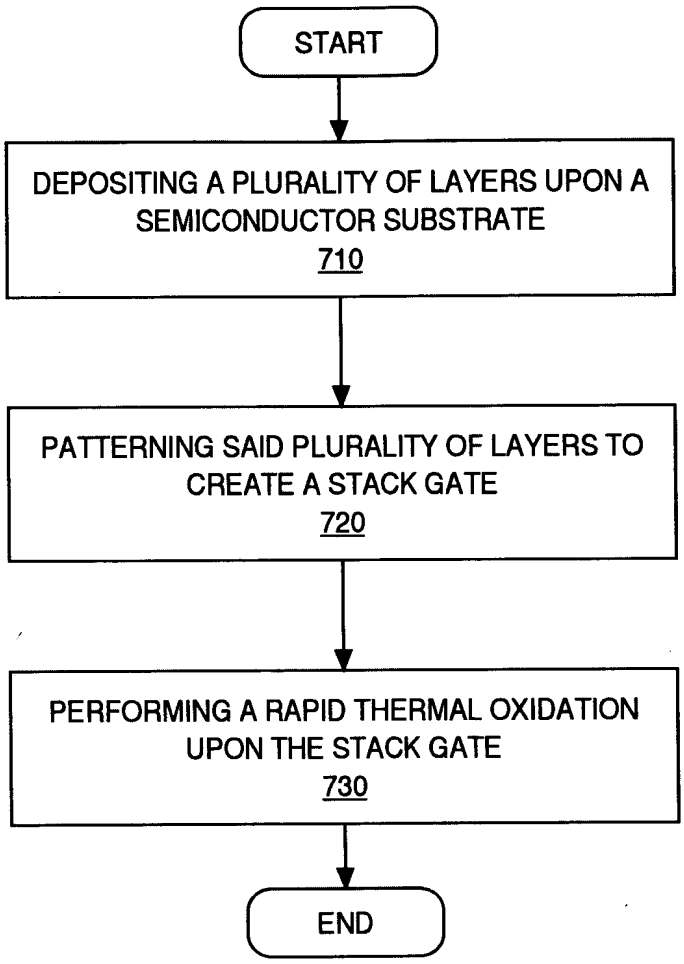
START
DEPOSITING A PLURALITY OF LAYERS UPON A SEMICONDUCTOR SUBSTRATE
710
PATTERNING SAID PLURALITY OF LAYERS TO CREATE A STACK GATE
720
PERFORMING A RAPID THERMAL OXIDATION UPON THE STACK GATE
730
END

FIGURE 7